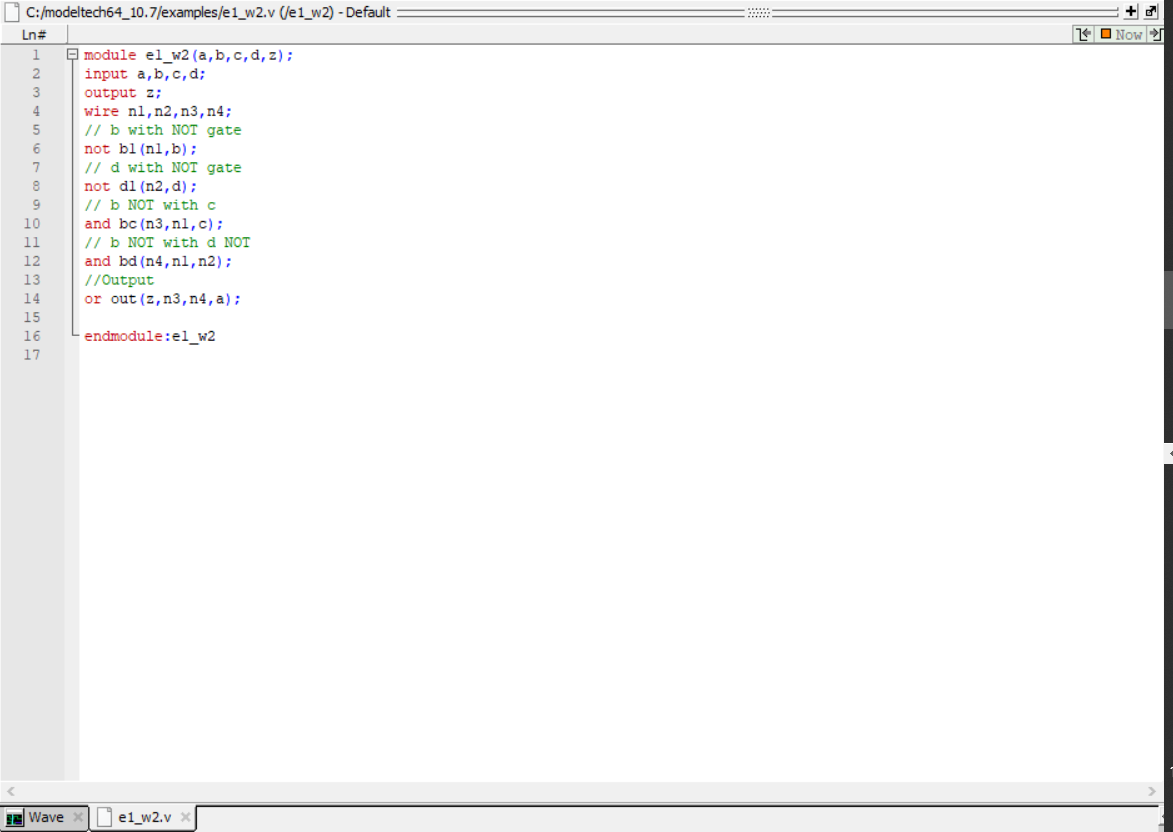
Ex 2

K-map

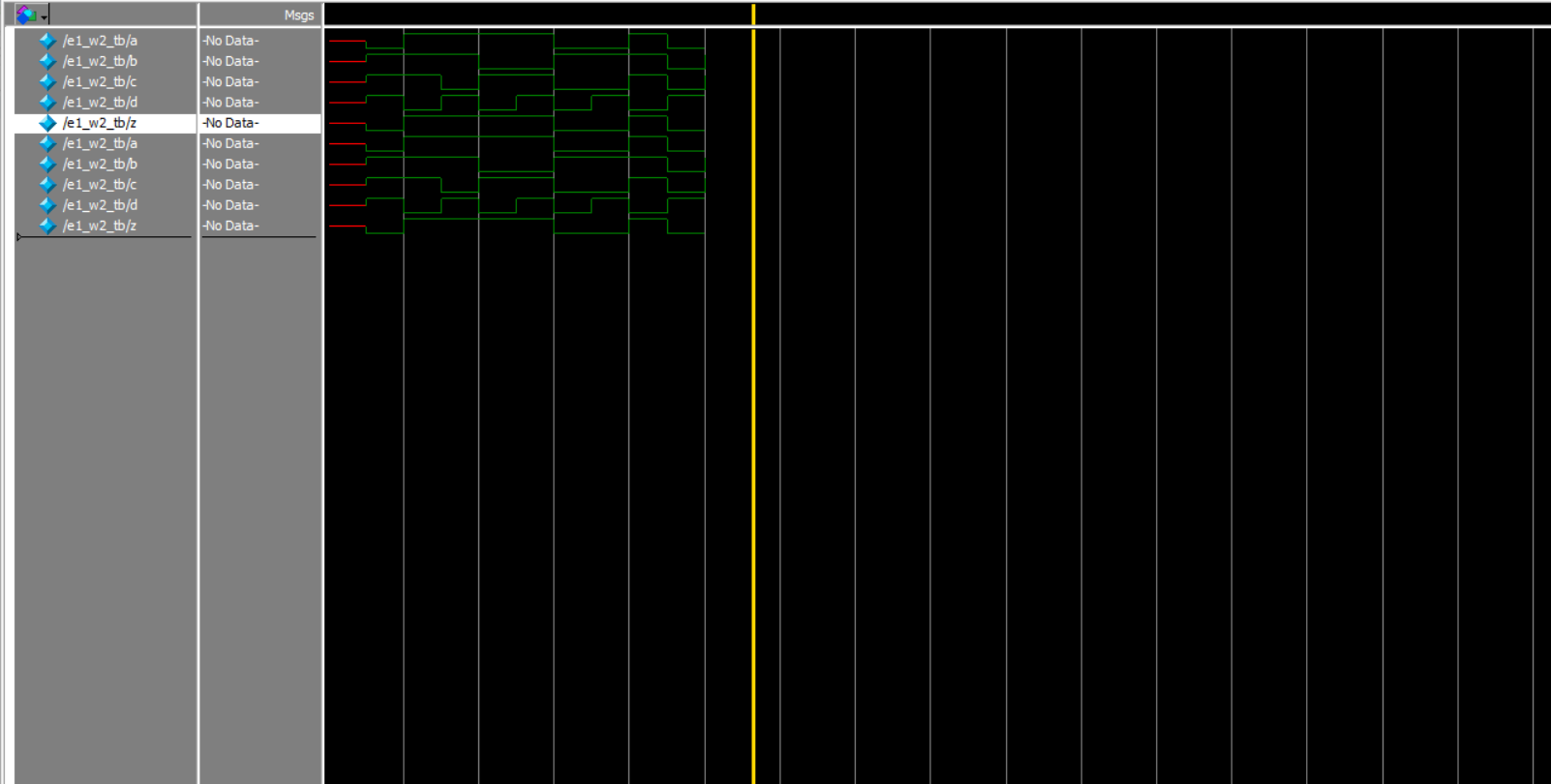
Verilog code



Testbench file

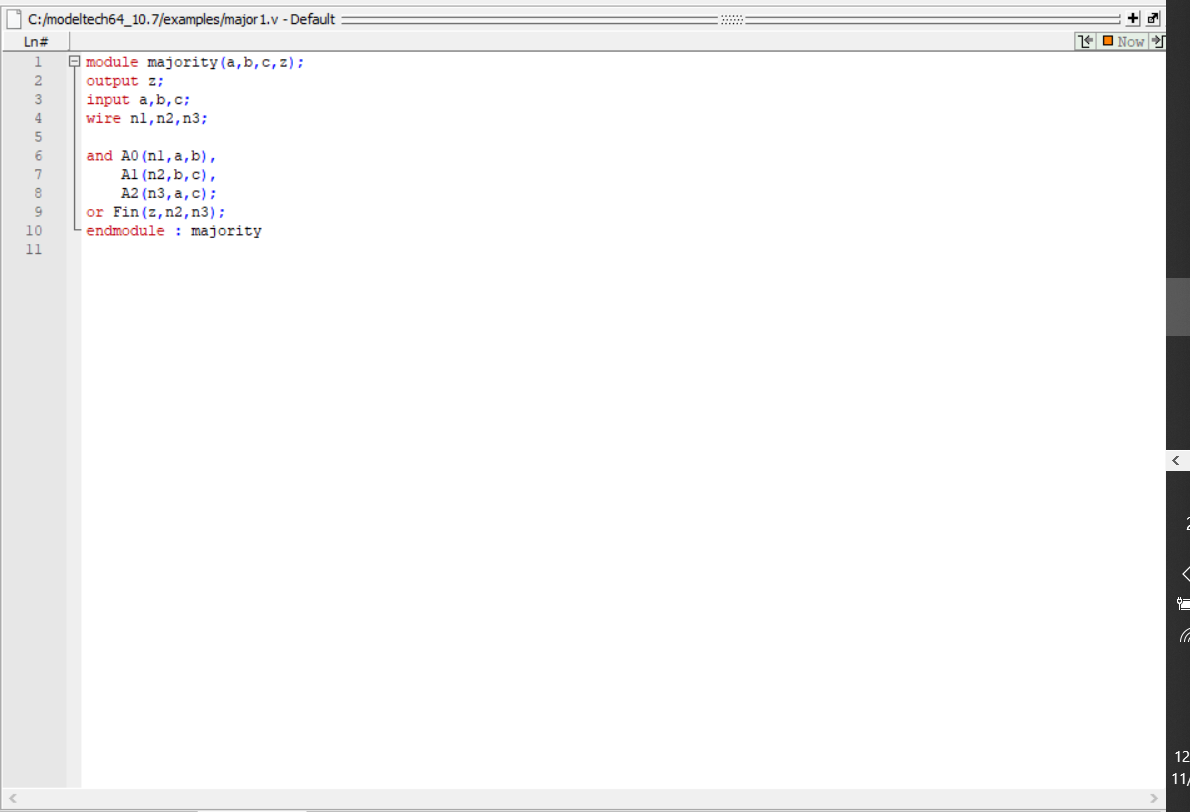


Wave simulation

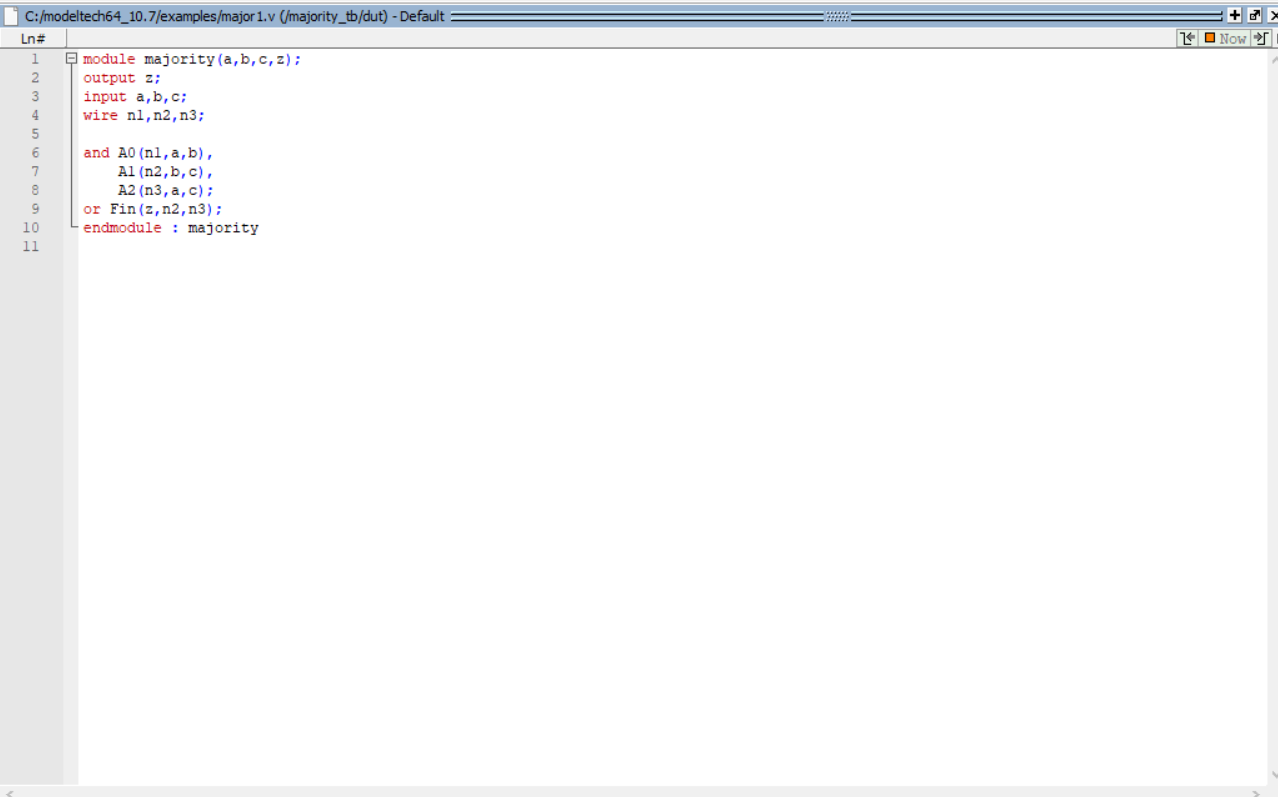


Majority

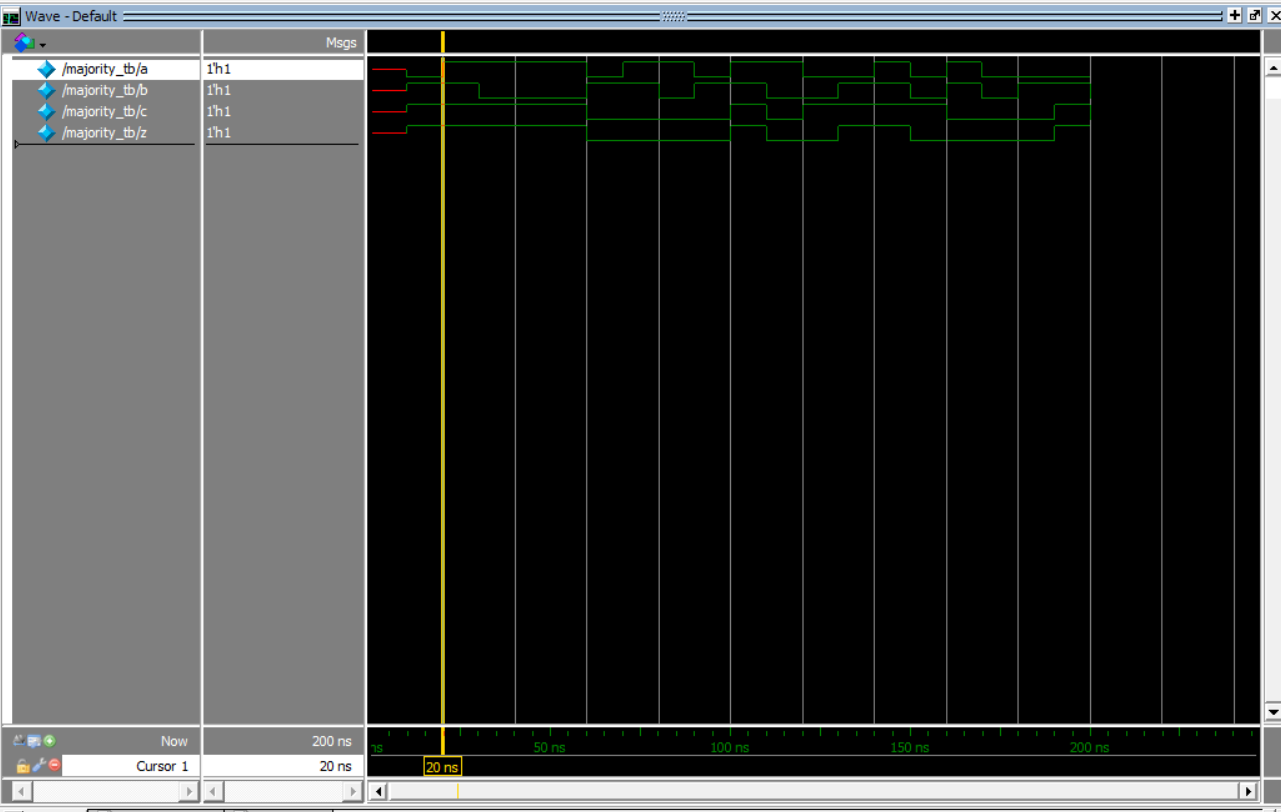
Verilog code



Testbench

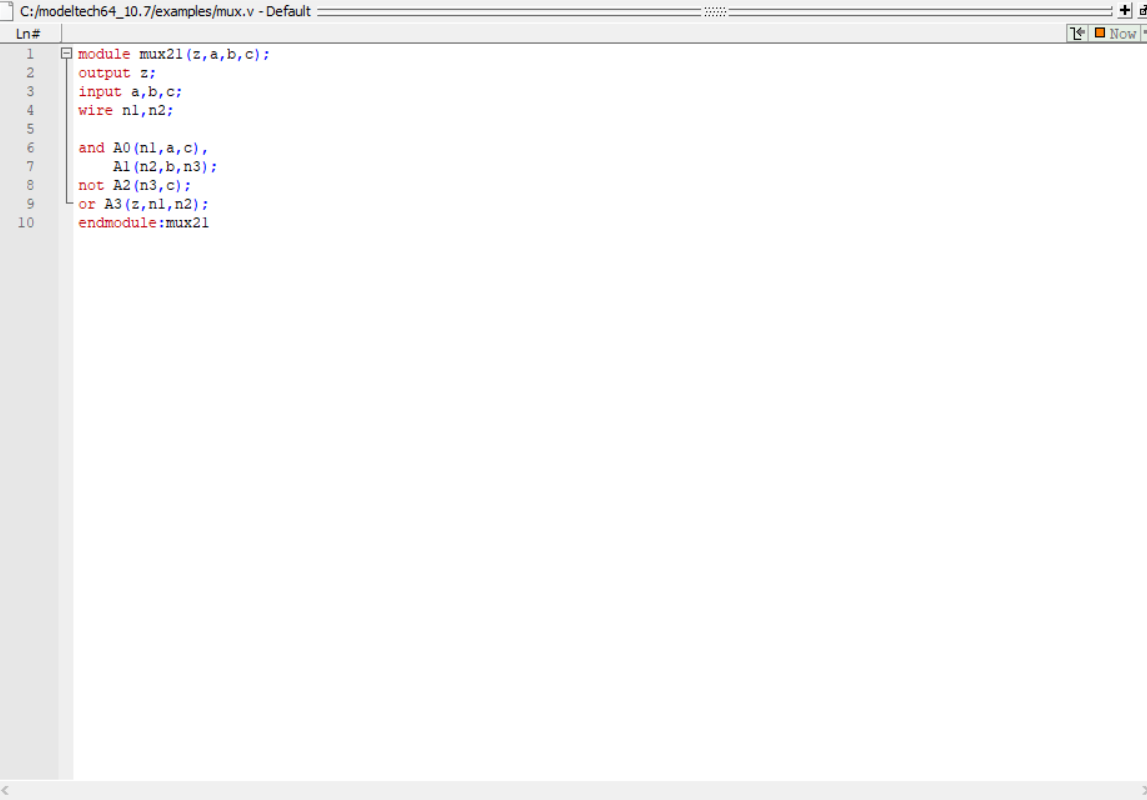


Wave simulation

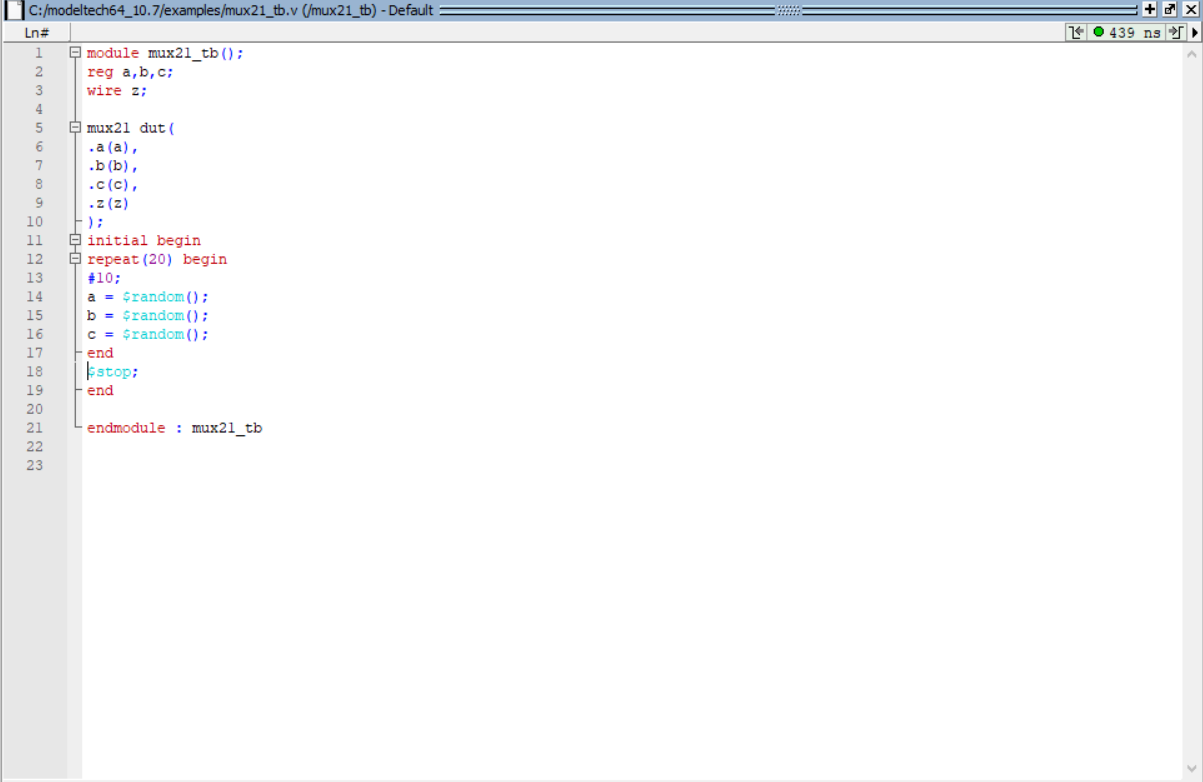


Mux 2x1

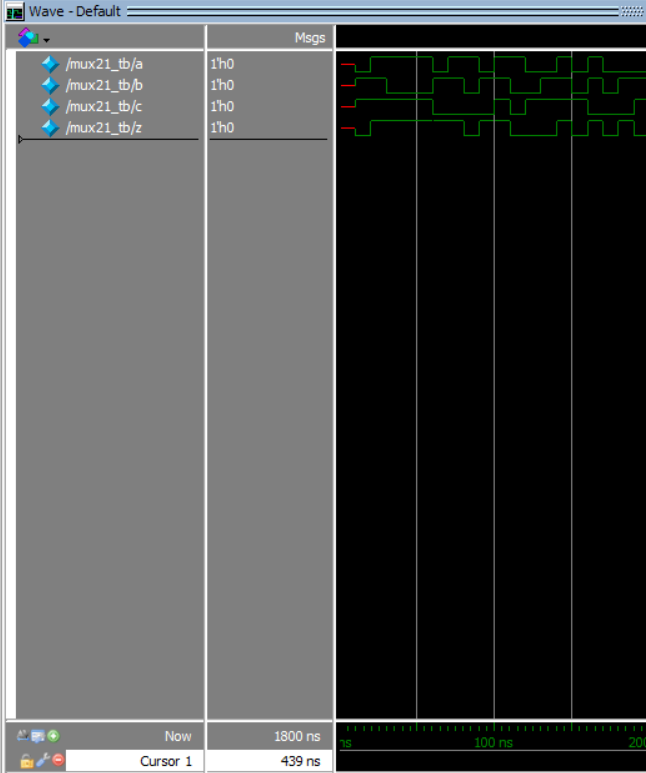
Verilog code



Testbench

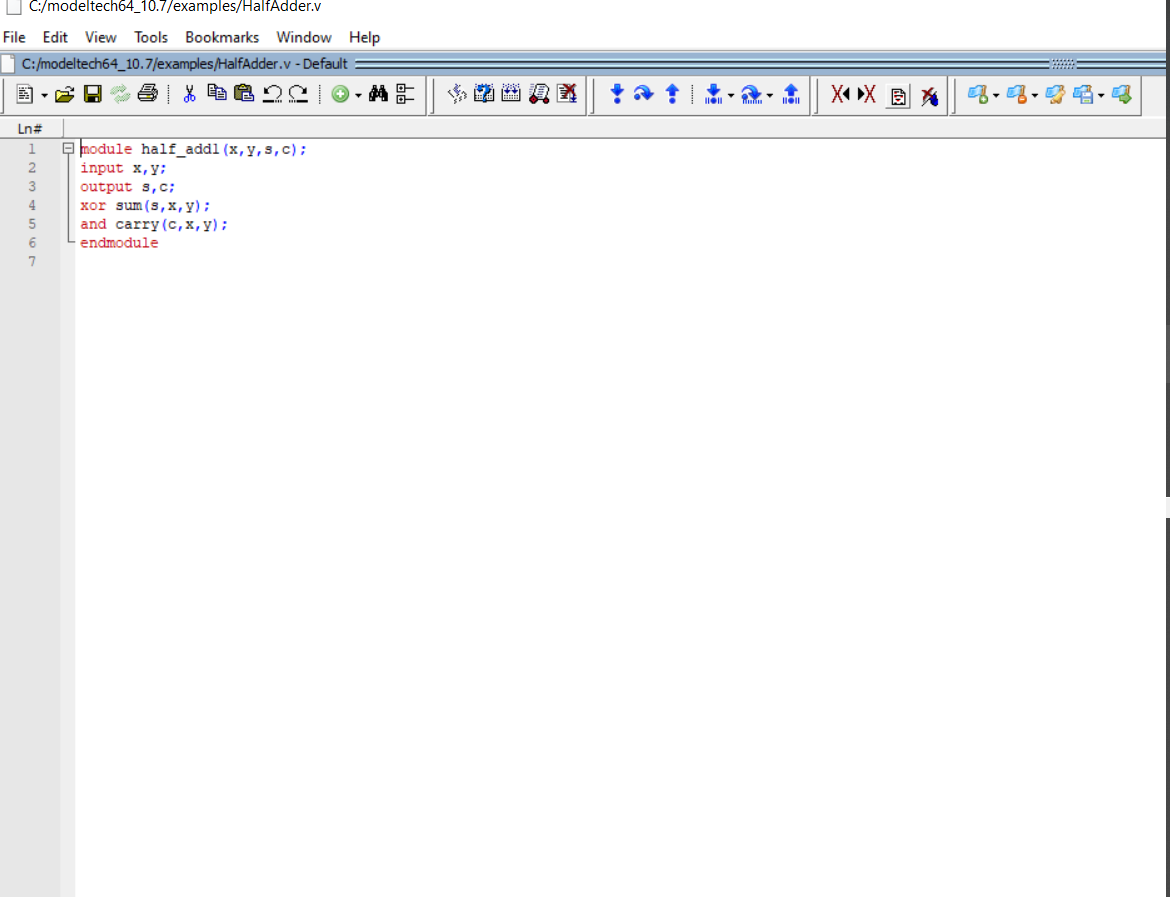


Wave simulation

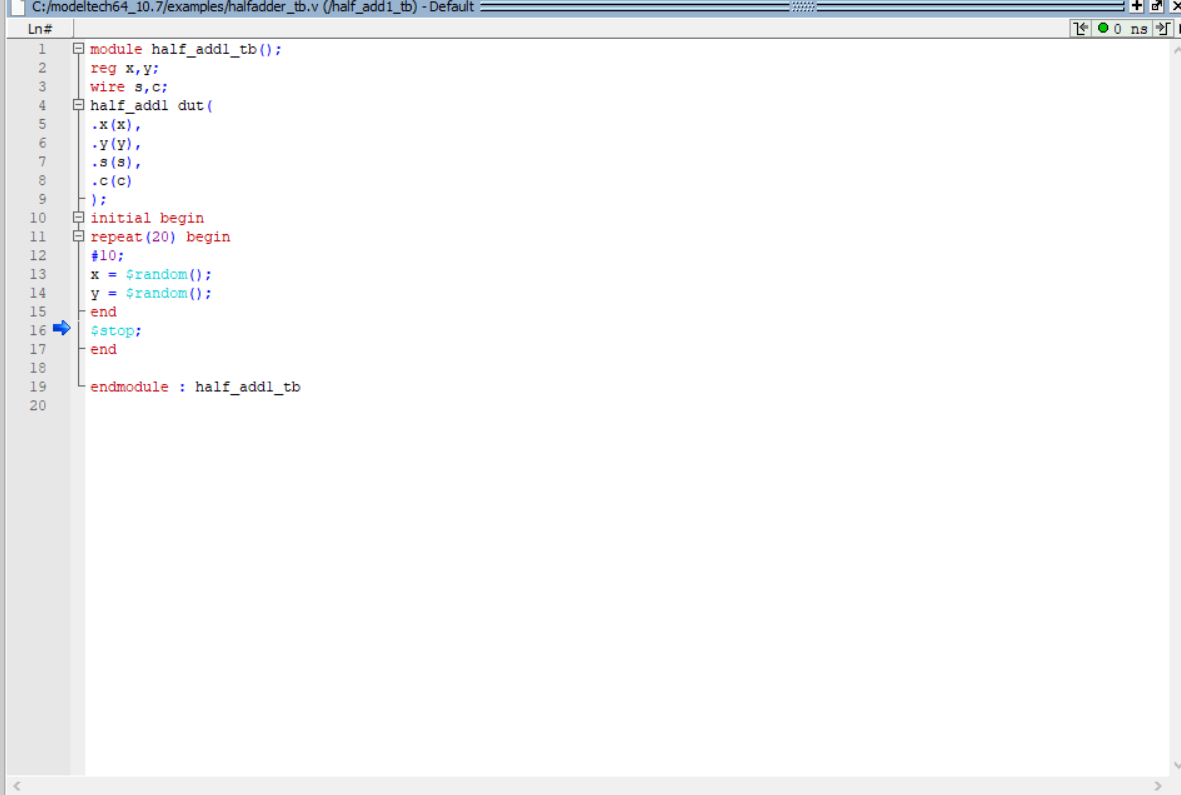


Half-adder

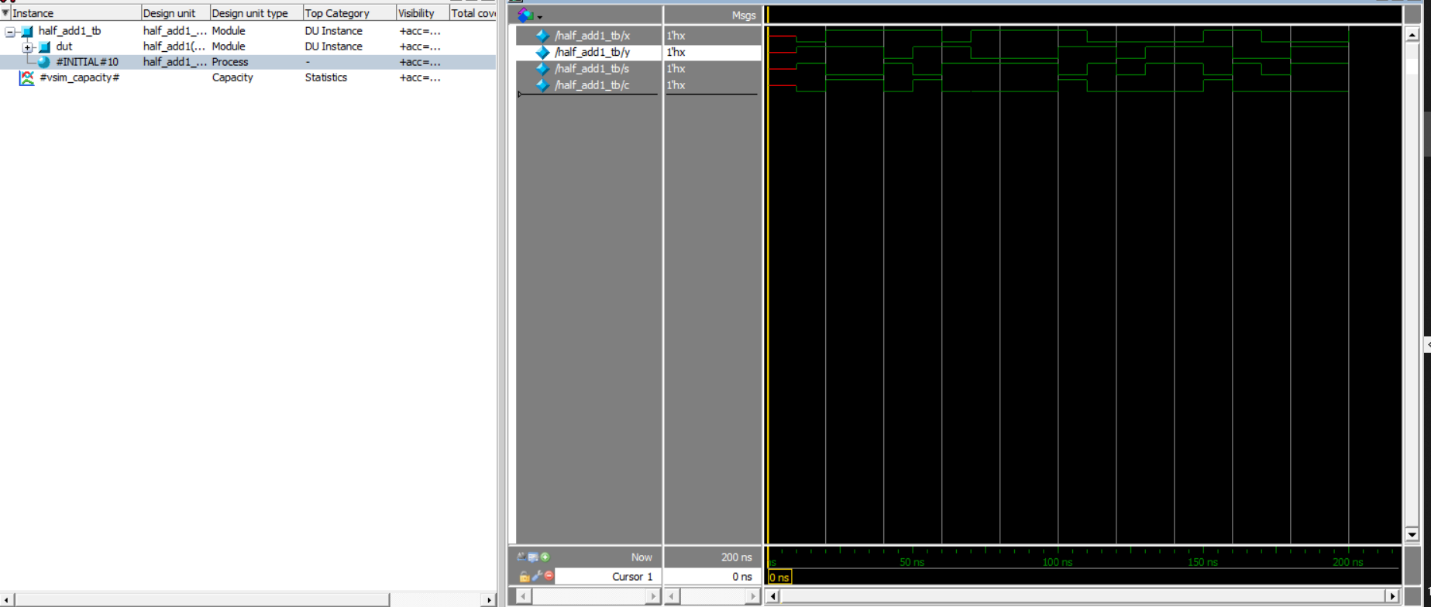
Verilog code



Test bench

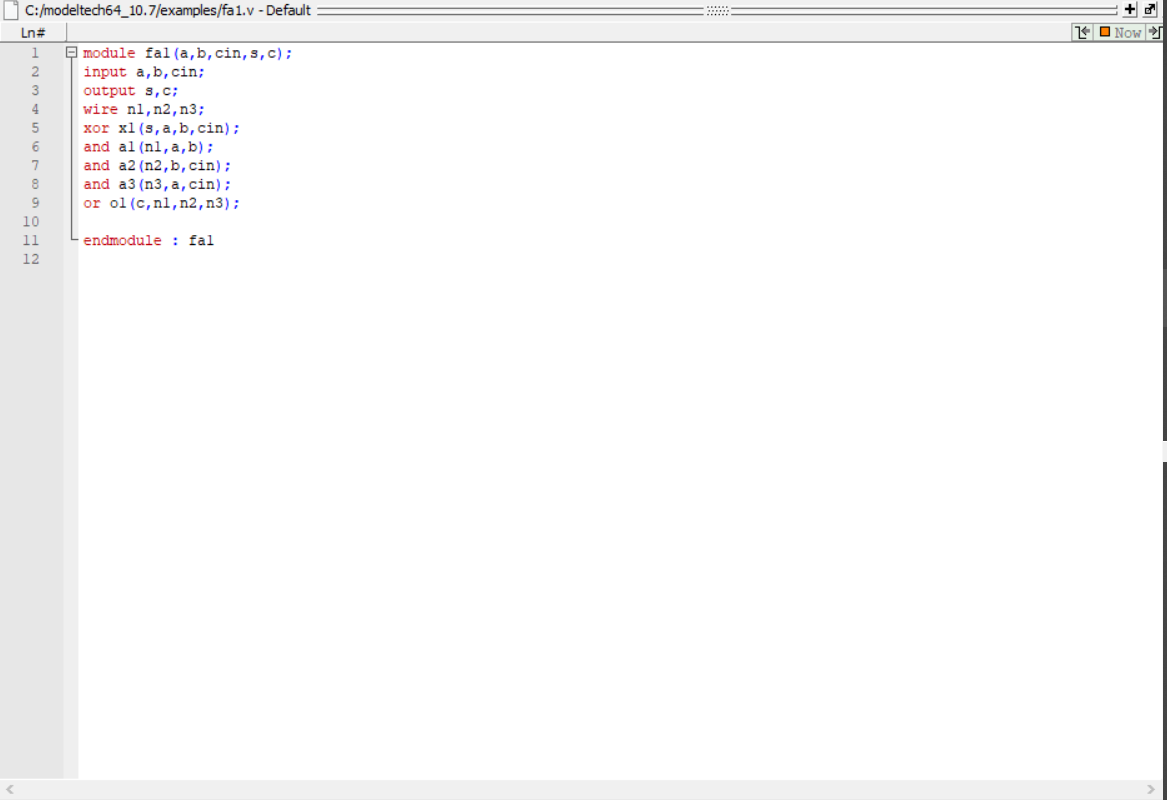


Wave simulation

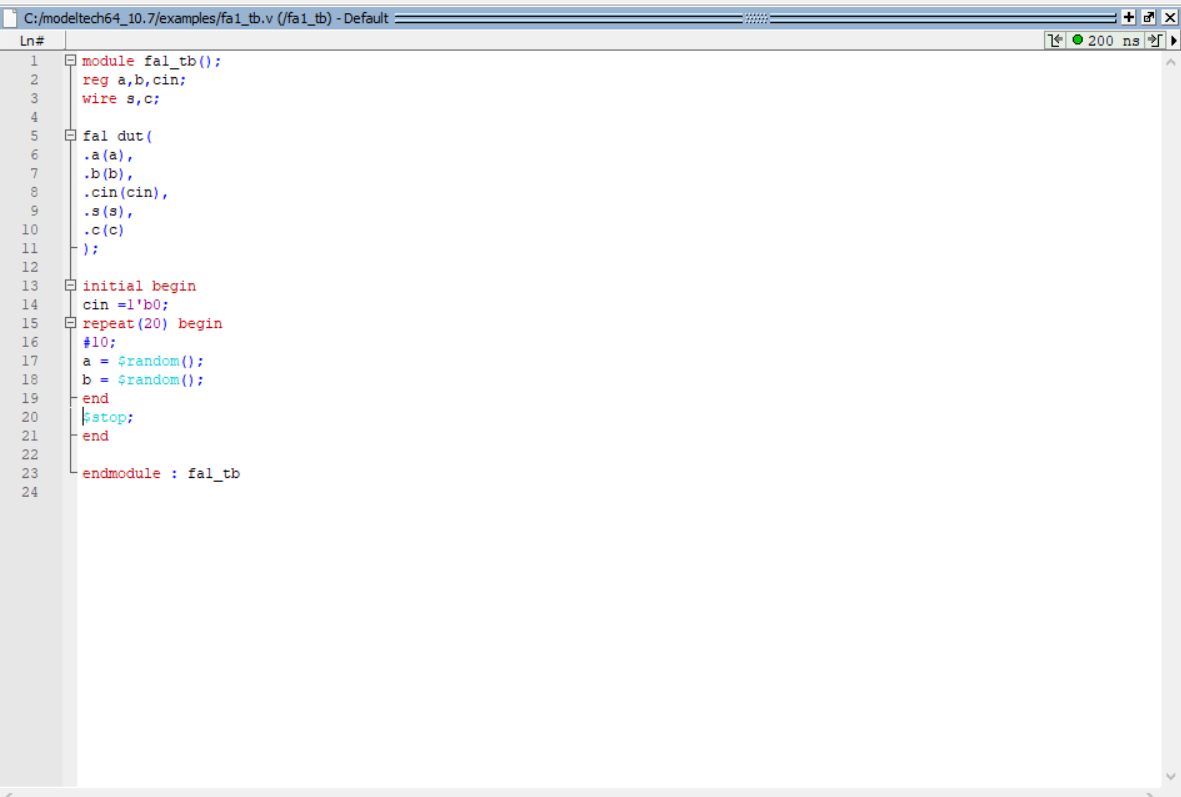


Full-adder

Verilog code



Testbench



Wave simulation

